CLAIMS

WHAT IS CLAIMED IS:

1. A method comprising:

allocating registers;

building a trace comprising basic blocks; and

scheduling instructions within said trace after said allocating registers.

2. The method of Claim 1 wherein said scheduling instructions comprises moving instructions between said basic blocks.

3. The method of Claim 1 further comprising building a control flow graph comprising said basic blocks.

4. The method of Claim 3 wherein said control flow graph comprises an off trace basic block.

5. The method of Claim 4 wherein said scheduling instructions comprises recognizing data dependencies from said off trace basic block.

6. The method of Claim 1 wherein said scheduling instructions comprises computing height information of said instructions.

7. The method of Claim 6 wherein said height information is computed using execution probabilities of said basic blocks.

8. The method of Claim 6 wherein said height information is computed using adjusted execution times of said instructions.

9. The method of Claim 1 wherein said scheduling instructions comprises computing an adjusted execution time of an instruction of said instructions by multiplying an execution time of said instruction by an execution probability factor.

10. The method of Claim 1 wherein said scheduling instructions comprises generating compensation code.

11. The method of Claim 1 wherein said scheduling instructions comprises:

building a trace block comprising said instructions;

scheduling said instructions within said trace block; and

moving said instructions from said trace block to said basic blocks.

12. A method comprising:

allocating registers;

building a trace after said allocating registers, said trace comprising basic blocks comprising instructions;

building a trace block comprising said instructions;

scheduling said instructions within said trace block; and

moving said instructions from said trace block to said basic blocks.

13. The method of Claim 12 wherein said building a trace block comprises inserting a join instruction into said trace block, said join instruction being a delimiter for a first basic block of said basic blocks.

14. The method of Claim 13 further comprising updating a use set of said join instruction with a global_live_in for an off trace basic block.

15. The method of Claim 14 wherein said global_live_in is a set of registers which contain live values when entering said off trace basic block.

16. The method of Claim 15 wherein an instruction of said instructions which defines a value in said set of registers is not moved past said join instruction during said scheduling said instructions.

17. The method of Claim 12 wherein said scheduling said instructions comprises computing height information of said instructions.

18. The method of Claim 17 wherein said height information is computed using execution probabilities of said basic blocks.

19. A system comprising:

a processor; and

a memory having a method of scheduling instructions therein, wherein upon execution of said method, said method comprises:

allocating registers;

building a trace comprising basic blocks; and

scheduling instructions within said trace after said allocating registers.

20. The system of Claim 19 wherein said scheduling instructions comprises moving instructions between said basic blocks.

21. The system of Claim 19 wherein said method further comprising building a control flow graph comprising said basic blocks.

22. The system of Claim 21 wherein said control flow graph comprises an off trace basic block.

23. The system of Claim 22 wherein said scheduling instructions comprises recognizing data dependencies from said off trace basic block.

24. The system of Claim 19 wherein said scheduling instructions comprises computing height information of said instructions.

25. The system of Claim 24 wherein said height information is computed using execution probabilities of said basic blocks.

26. The system of Claim 24 wherein said height information is computed using adjusted execution times of said instructions.

27. The system of Claim 19 wherein said scheduling instructions comprises generating compensation code.

28. A computer system comprising:

means for allocating registers;

means for building a trace comprising basic blocks; and

means for scheduling instructions within said trace after said registers are allocated by said means for allocating.

29. A computer program product having a method of scheduling instructions stored therein, wherein upon execution of said method, said method comprises:

allocating registers;

building a trace comprising basic blocks; and

scheduling instructions within said trace after said allocating registers.